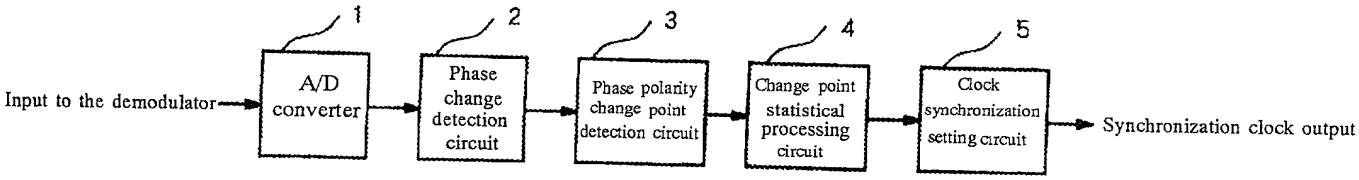

Input to the demodulator
1
A/D converter
2
Phase change detection circuit
3
Phase polarity change point detection circuit
4
Change point statistical processing circuit
5
Clock synchronization setting circuit
Synchronization clock output

Fig. 1

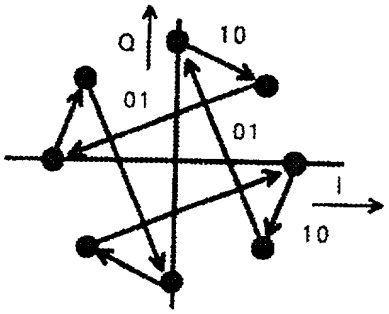


Fig. 2

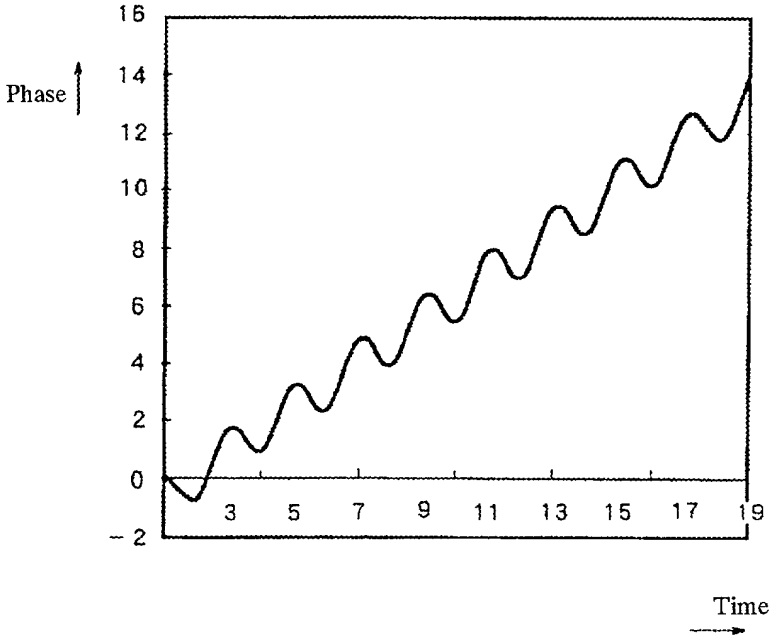


FIg. 3

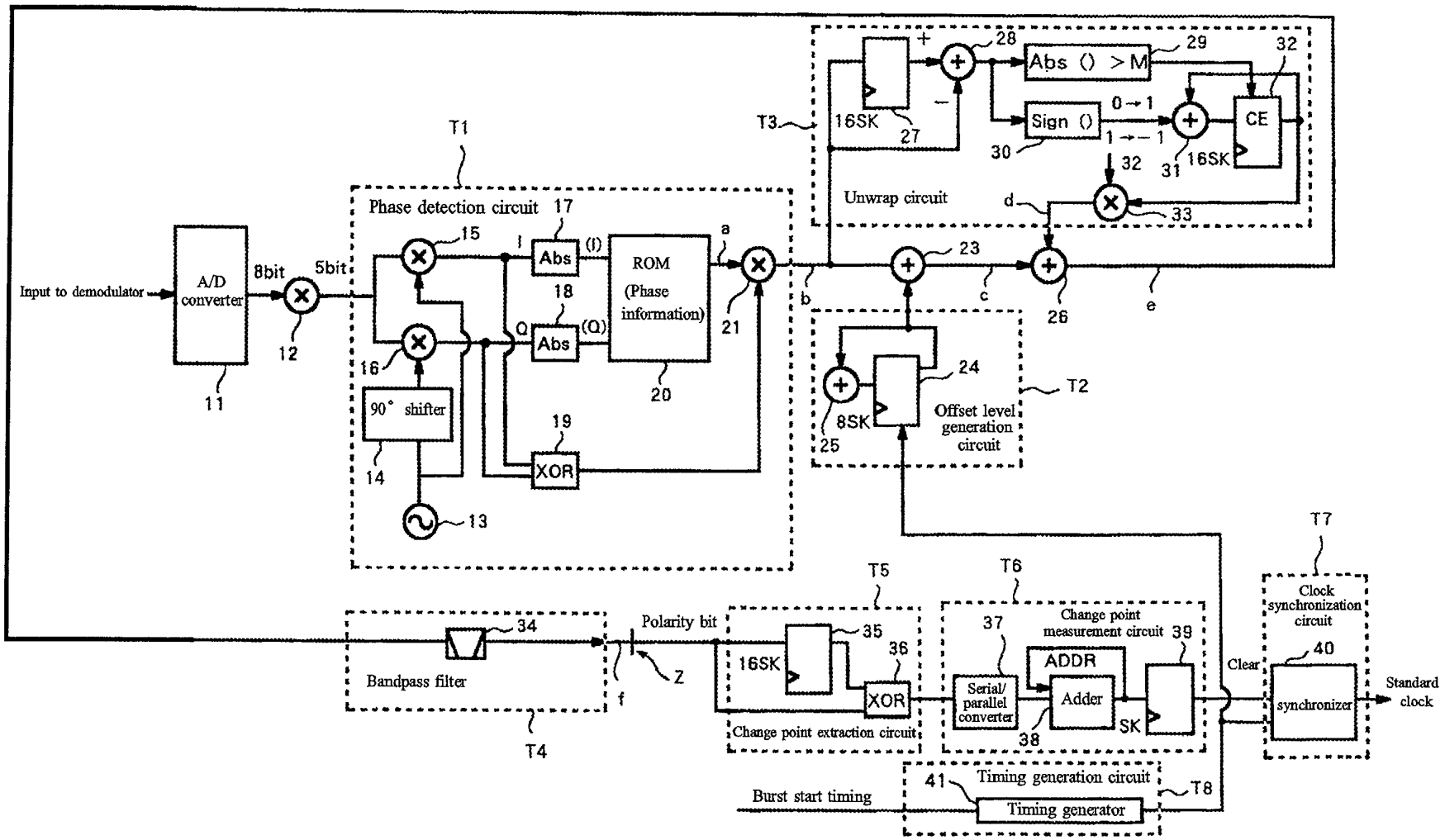
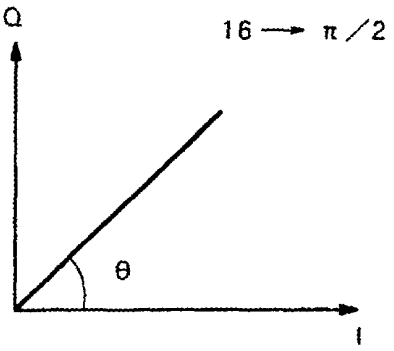

Input to demodulator
A/D converter
11
8bit
5bit
12
T1
Phase detection circuit
17
15
16
90° shifter
14
13
I
Q
Abs
(I)
18
Abs
(Q)
19
XOR
ROM
(Phase information)
20
a
21
T3
16SK
27
28
Abs () >M
29
32
Sign ()
30
0→1
1→−1
31
16SK
CE
32
Unwrap circuit
d
33
b
23
c
26
e
T2
8SK
25
24
Offset level generation circuit
T7
Clock synchronization circuit
40
Clear
synchronizer
Standard clock
T5
T6
Change point measurement circuit
37
39
ADDR
Serial/ parallel converter
Adder
SK
38
34
Bandpass filter
T4
Polarity bit
f
Z
16SK
35
36
XOR
Change point extraction circuit
Burst start timing
41
Timing generation circuit
Timing generator
T8

Fig. 4

(a)

Q \ I	0000	0001	0010	・ ・ ・
0000	a1	a2	a3	・ ・ ・
0001	a4	a5	a6	・ ・ ・
0010	a7	a8	a9	・ ・ ・
・	・	・	・	・
・	・	・	・	・
・	・	・	・	・

(b)



(c)

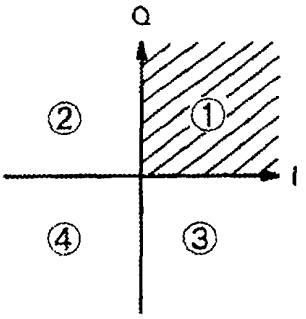


Fig. 5

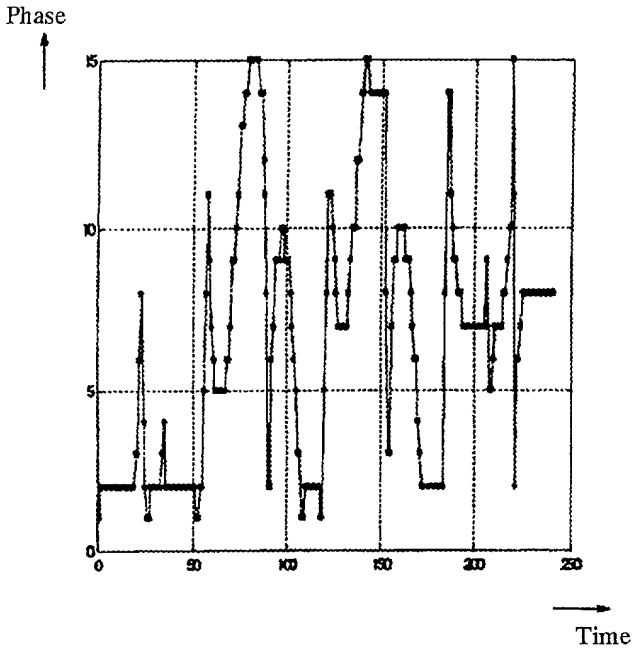


Fig. 6

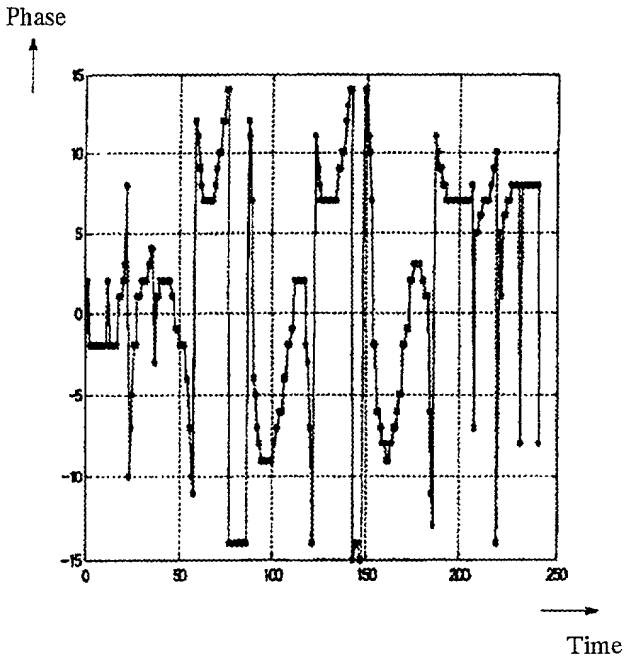


Fig. 7

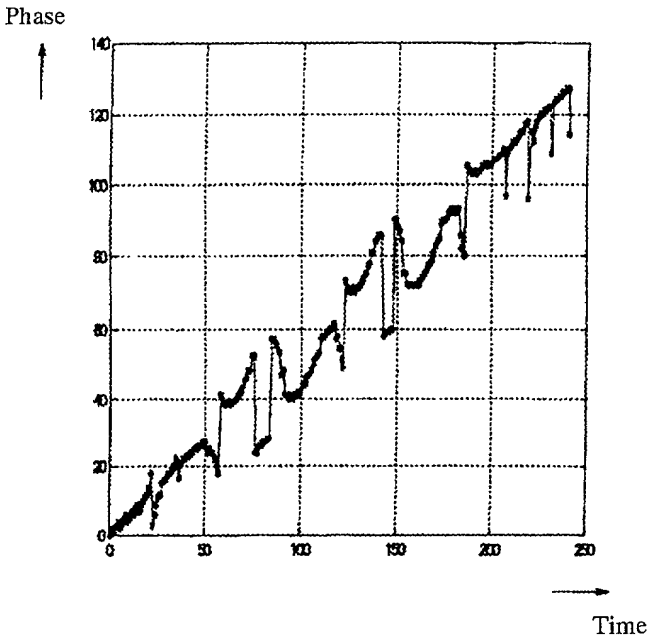


Fig. 8

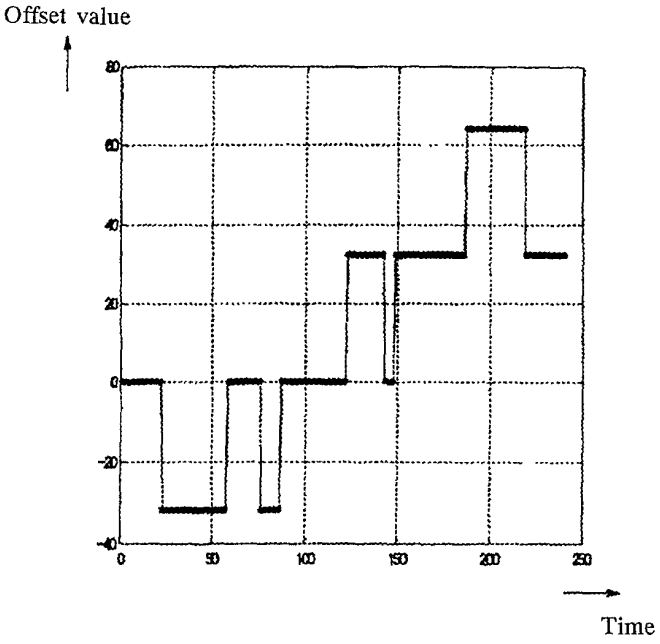


Fig. 9

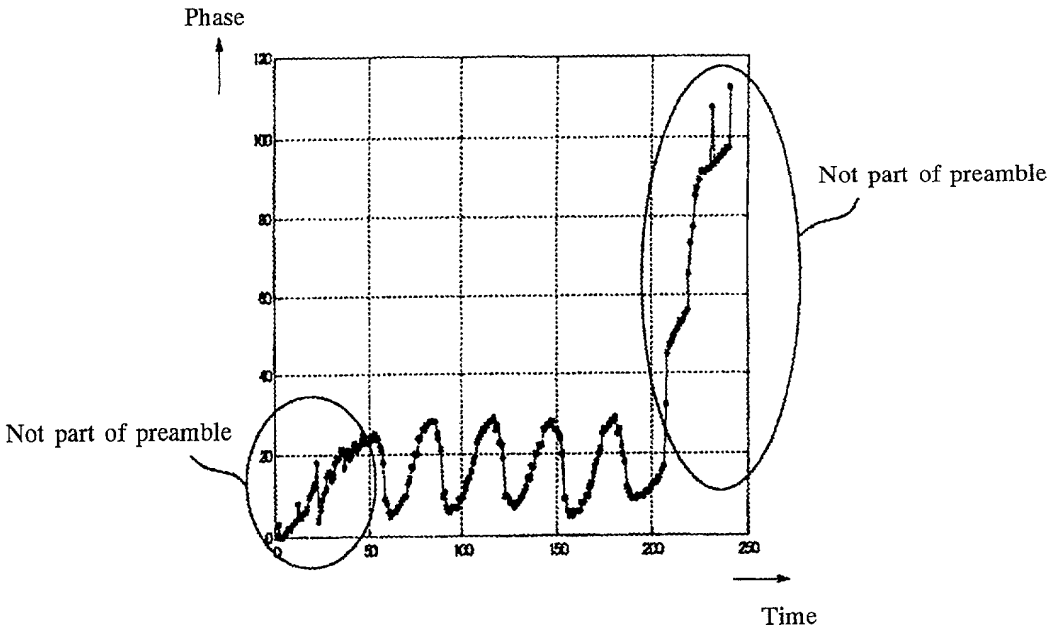


Fig. 10

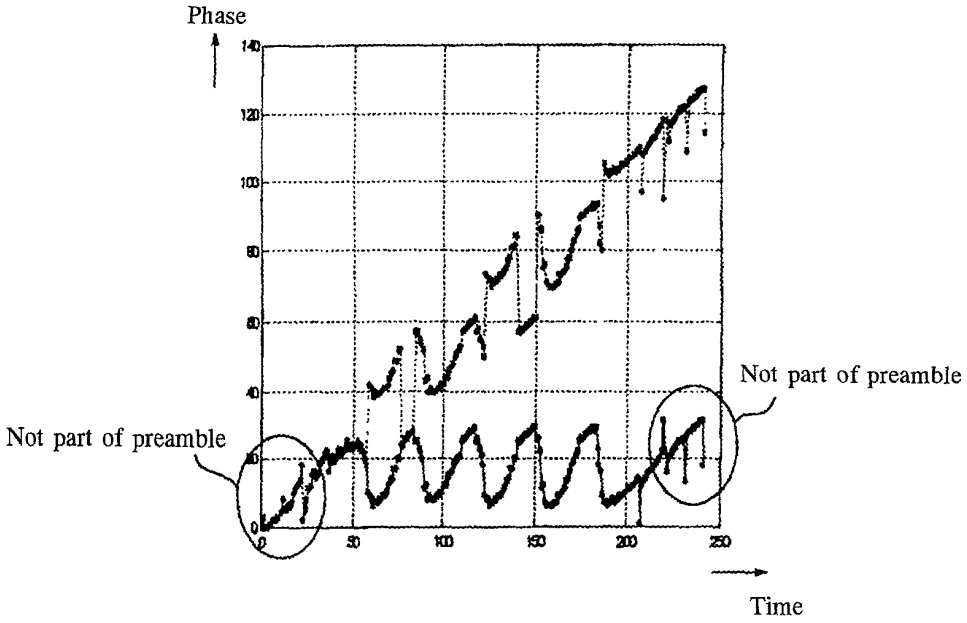


Fig. 11

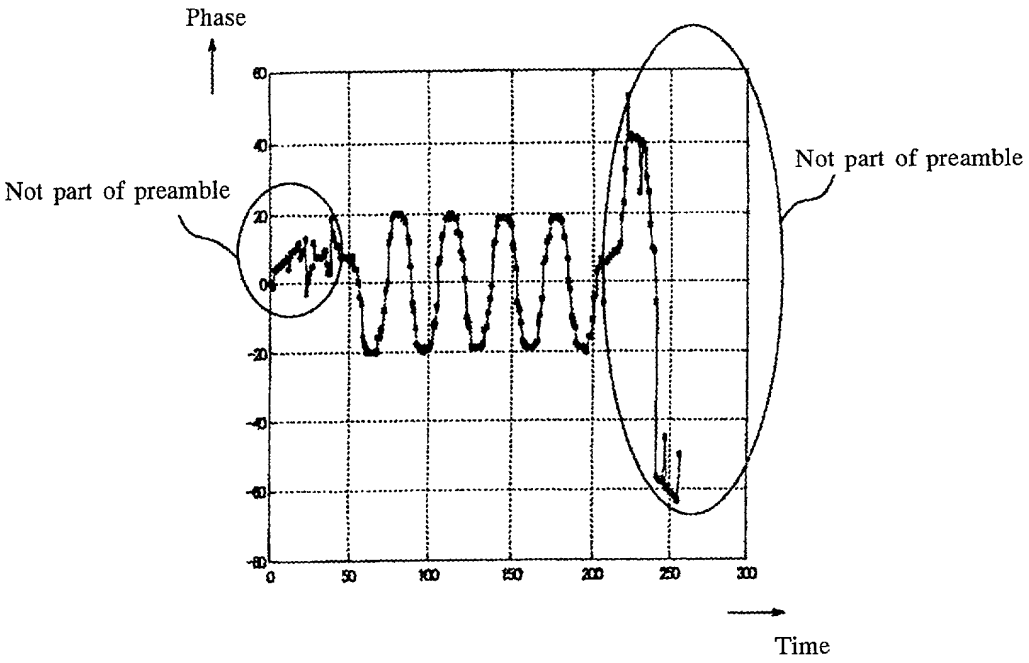

Phase
Not part of preamble
Not part of preamble
Time
60
40
20
0
-20
-40
-60
-80
0
50
100
150
200
250
300

Fig. 12

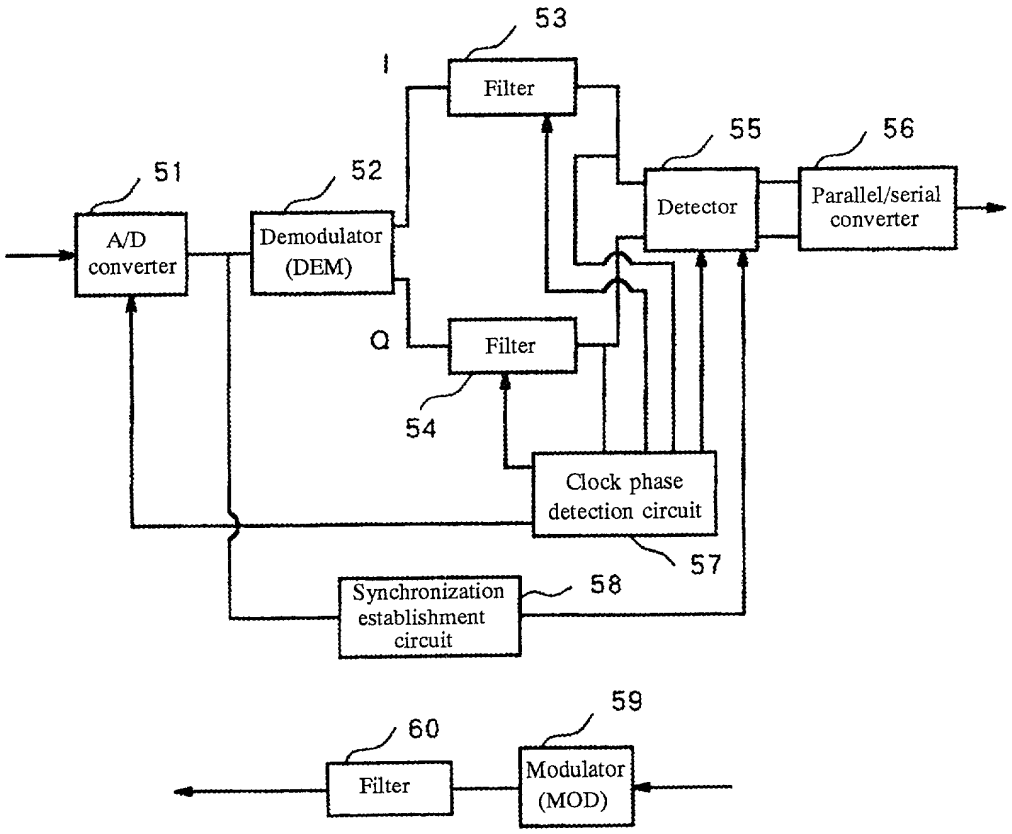
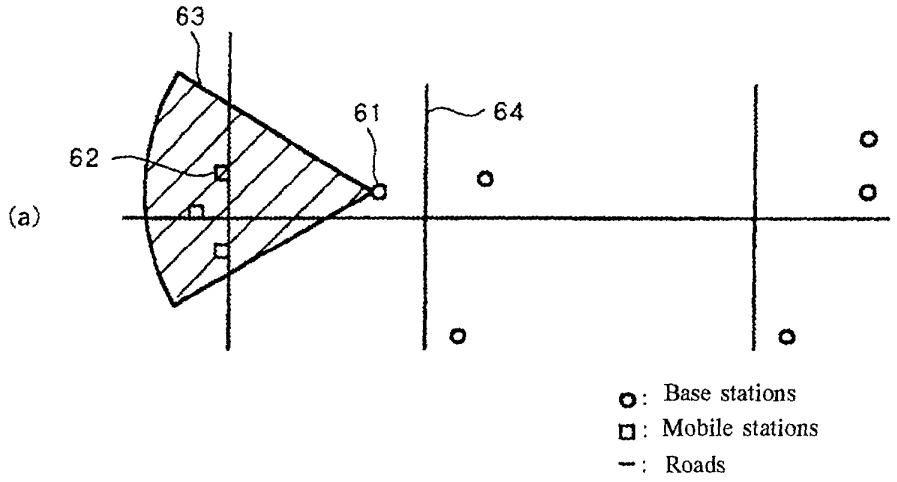

53
I
Filter
55
56
51
52
Detector
Parallel/serial converter
A/D converter
Demodulator (DEM)
Q
Filter
54
Clock phase detection circuit
57
Synchronization establishment circuit
58
59
60
Filter
Modulator (MOD)

Fig. 13


63
61
64
62
(a)
: Base stations
: Mobile stations
: Roads

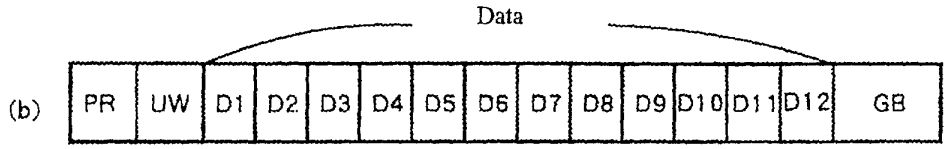

Data
(b)
PR
UW
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
GB

Fig. 14

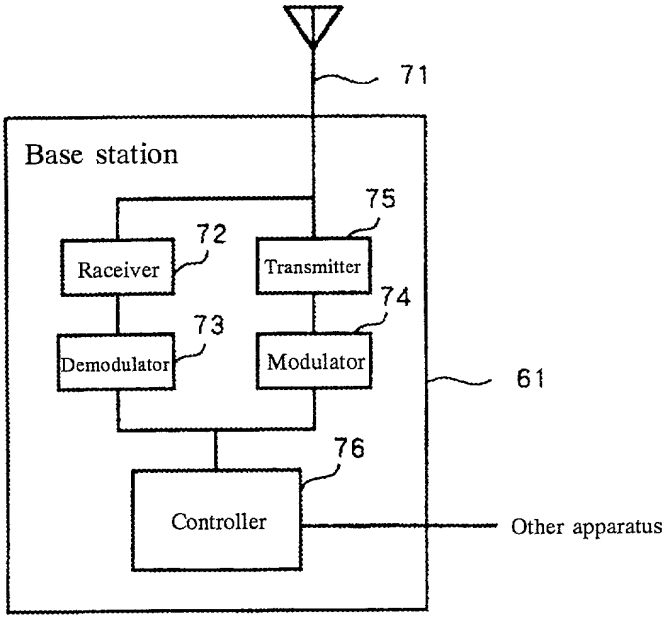
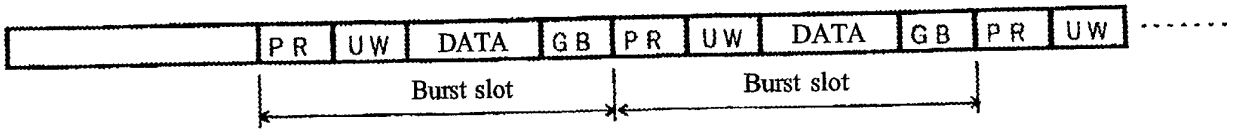

71
Base station
75
72
Raceiver
Transmitter
74
73
Demodulator
Modulator
61
76
Controller
Other apparatus

Fig. 15



PR : Preamble pattern

UW : Unique word (identification pattern)

DATA : Body of communications data

GB : Gurd bits (buffer timing between slots)

Fig. 16

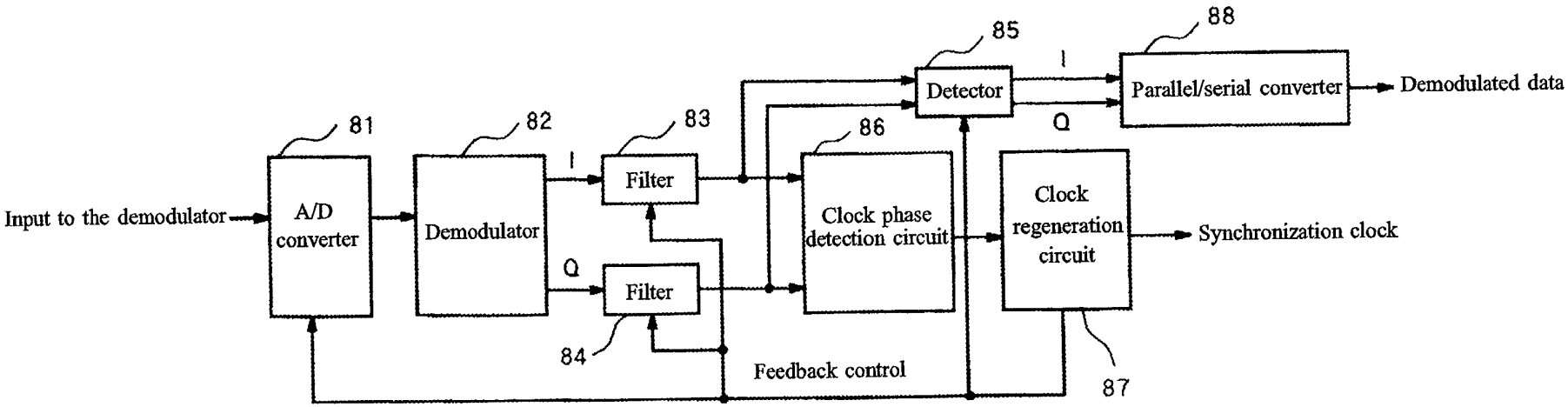
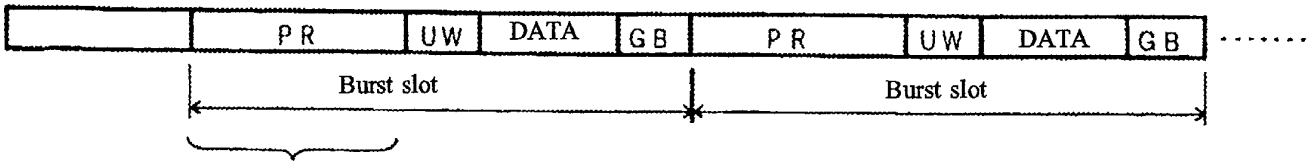

Input to the demodulator
A/D converter
81
Demodulator
82
I
Q
Filter
83
Filter
84
Clock phase detection circuit
86
Detector
85
I
Q
Parallel/serial converter
88
Demodulated data
Clock regeneration circuit
87
Synchronization clock
Feedback control

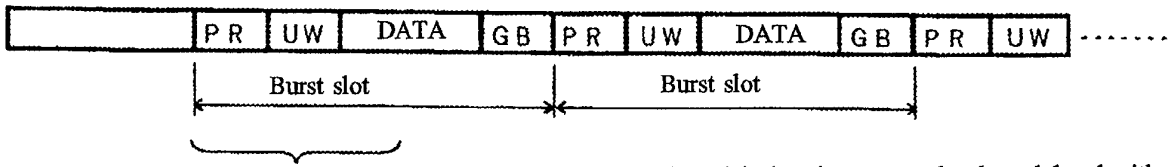
Fig. 17

(a) Case in which preamble is lengthened



Preamble period is made 100 symbols or longer
In this case, the length of the preamble becomes a large fraction of the entire length, so the data transmission rate drops.

(b) Case in which first burst is discarded



If the preamble is not made long, there is a risk that data cannot be demodulated with only a length of roughly 100 symbols. In the above diagram, there is a risk that the portion up to UW and DATA cannot be received correctly at the time of receipt of the first burst. In addition, it is necessary to hold the timing of synchronization at the time of receipt of the first burst so that it can be used in the second and subsequent bursts.

PR : Preamble pattern
UW : Unique word (identification pattern)
DATA : Body of communications data
GB : Guard bits (buffer timing between slots)

Fig. 18